IP-16ADC

User's Manual

16-bit, 16 Channel
Analog to Digital Converter
IndustryPack®

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IP-16ADC

16-bit, 16 Channel Analog to Digital Converter IndustryPack®

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Table of Contents

List of Figures

Product Description

The IP-16ADC is part of the IndustryPack® family of modular I/O components. It provides 16 single-ended input lines or eight differential input lines. The single-ended and differential inputs may be dynamically mixed. The IP-16ADC provides 16 bits of resolution. Software programmable gains of 1 or 1/2 are provided along with software programmable modes of unipolar and bipolar. These two gains and two modes provide four input voltage ranges: 0 to 5, ±5, 0 to 10, and ±10.

A very high precision on board voltage reference is used to provide exceptional stability. Software triggered auto-calibration provides a basic accuracy of plus or minus one LSB (least significant bit).

A track and hold circuit internal to the A/D IC ensures accurate measurement of time varying signals. The IP-16ADC automatically changes from tracking to hold mode as each conversion is started. The tracking slew rate and accuracy may be controlled by software.

IP-16ADC conversion time is eight microseconds for the standard grade IP-16ADC. This provides a usable throughput rate of up to 100,000 conversions per second. The IP-16ADC has two conversion modes: Single and Continuous Conversion. In Single Conversion mode an A/D conversion is started by a write to a unique address in the I/O space and its completion is detected either by polling the Ready (SDL*) bit or by an interrupt.

In Continuous Conversion mode the first conversion is started by a write to a unique address in the I/O space. Subsequent conversions are initiated automatically after the end of the previous conversion. Each conversion completion may be detected either by polling the Ready (SDL*) bit or by an interrupt. Continuous mode is accessed by setting the control register FREERUN* bit to 0. Continuous mode is not the same as the Free Run mode described in the data sheet for the A/D converter IC. The A/D converter always runs in “Synchronous Self-Clocking” mode. When Continuous mode is enabled, a state machine on the IP periodically generates a HOLD pulse to trigger conversions. Conversions continue at a rate of one conversion every 9 microseconds regardless of whether data is read. This allows the IP-16ADC to continuously update the data register without software overhead thereby facilitating software access only when data is needed. Software can always determine the status of the A/D converter by examination of an A/D status bit. This pipelining has the advantage that the processor and the IP-16ADC can both be working at the same time to provide higher total throughput. Operation in Continuous mode requires careful programming to avoid reading the data register while it is being updated. Data should be read immediately after a Data Available interrupt or immediately after the SLD* bit changes from 0 to 1. The SDL* bit is a 1 for about 2 microseconds between conversions.

An external hardware acquisition trigger input on the I/O interface can be used to trigger either mode of conversion. Typically a precision external timing circuit synchronized with the events to be measured is used to drive this input. The user must coordinate this circuit with the software accessing the IP-16ADC. Prior to starting a conversion, the control register must be set up to the desired input configuration, channel number, A/D gain, A/D polarity, conversion mode and the various settling times must be met. When driving the external conversion request, the conversion trigger line must be released following the start of the conversion so that a new sample may be tracked.

A single 16-bit read/write control register controls the input configuration, channel, A/D gain, A/D polarity, conversion mode, A/D reset, interrupt enables and reports status. Most of the bits have “read back” capability so multiple routines can share access to the board while verifying the

current configuration. Both 8-bit and 16-bit read cycles are supported; however, only 16-bit (word) write cycles may be used to update the control register.

The IP-16ADC conforms to the Industry Pack Interface Specification Revision 0.7. This guarantees compatibility with the various carrier boards, busses and form factors. This compatibility permits application code migration between otherwise incompatible systems and therefore provides for a longer life of the customer's software investment.

Shown below in Figure 1 is the simplified block diagram of the IP-16ADC.

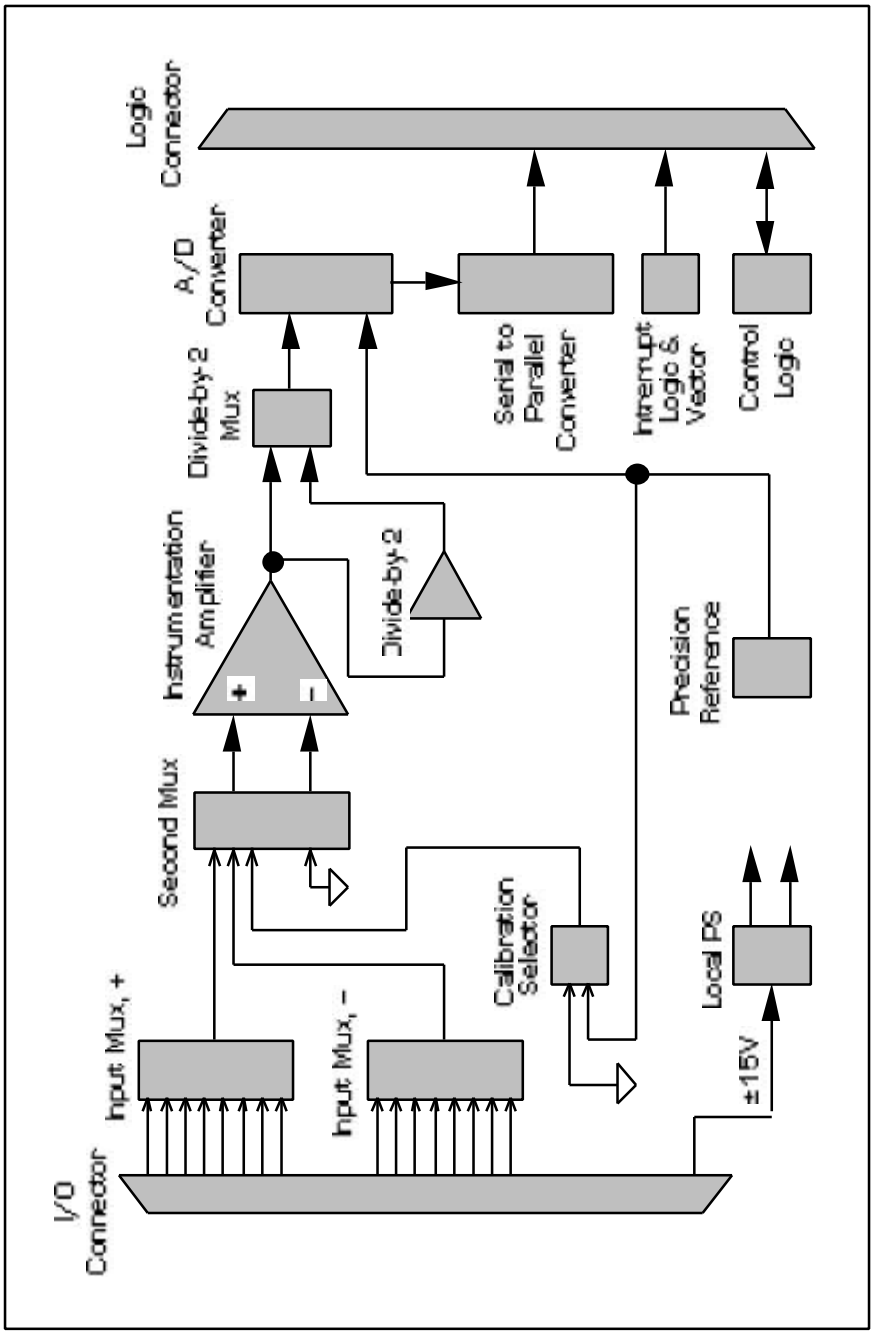

Figure 1 IP-16ADC Block Diagram

Connection to the IP-16ADC is through a standard 50-conductor ribbon cable. This cable may be terminated in a 50 position screw terminal block, available from GreenSpring Computers and other manufacturers, or any user-determined hardware. The IP-16ADC Engineering Kit includes a cable and terminal block.

All of the IP-16ADC inputs are alternated on the cable with double analog grounds. The double grounds provide significantly better isolation between inputs than single grounds. Differential inputs are on conductors three wires apart. This short spacing (approximately 0.300 inches) minimizes any differential temperature effects that could reduce the accuracy of a reading by introducing unwanted thermocouple voltages.

The two software programmable gain settings of 1 or 1/2 provide for direct input of a range of sensors and instrumentation. Both input ranges provide for symmetric bipolar or unipolar input. This means that polarities do not have to be observed when connecting sensors. Signal input over-voltage protection of ±35 volts is provided. This protection is provided by the input multiplexer ICs.

IP-16ADC is designed for very high accuracy conversion of multiple analog signals. It implements 16 single-ended or 8 differential 16-bit analog-to-digital conversion channels. Dynamic calibration from a low drift internal reference is supported. The ADC device includes auto-calibration.

Internal amplification and buffering is implemented with very low distortion differential amplifiers. Typical linearity is 0.001%. The internal reference has a temperature drift coefficient of 2 ppm/°C maximum. Internal calibration is accurate to better than ±2 LSB. See the Specifications at the end of this Manual for more details.

The IP-16ADC achieves a resolution of 16 bits at a throughput rate of 100 KHz.

Input circuitry consists of a multiplexer group feeding a low noise, low distortion instrumentation amplifier. Input impedance is 60 M? . Common mode rejection ratio is 91 db at 60 Hz. The multiplexers include built-in over voltage protection to ±35 volts.

Internal calibration uses the following capabilities: (1) auto-calibration of ADC, (2) reading of analog ground voltage, (3) reading of the voltage reference, (4) reading of the voltage reference divided by two. This permits accurate measurement of the offset error (zero volt) and the gain error (full scale or half scale). These errors are introduced by the instrumentation and gain amplifiers. These errors are removed in software, included as part of GreenSpring's Driver. Even the uncalibrated accuracy of the IP-16ADC is quite high; it is affected primarily by the 10 ppm/°C gain drift (maximum) of the instrumentation amplifier.

Programmable interrupt logic is provided to generate an interrupt when a conversion is completed. Start of conversion may be initiated by a software command or by an external trigger. An external pacer clock may be used to provide a semi-automatic data acquisition capability (interrupt per sample). Maximum aggregate conversion rate is 100 KHz.

Full scale input voltage ranges are 0 to 5, ±5, 0 to 10 and ±10 volts.

VMEbus Addressing

The address map of the IP-16ADC on the VMEbus is given below in the Figure. All addresses are in IP I/O space. Byte accesses are on data lines D7..D0. Word accesses are on D15..D0.

Register Name	68K Address	Access
Control and Status	$00	Word, R/W
A/D Data Reg	$04	Word, R
Vector Reg	$09	Byte, R/W
Conversion Req Trig	$0C	any, W

2 VMEbus Address Map

See section Programming below for register details.

Interrupt mapping is a function of the selected carrier board. See your IP carrier board User Manual for more information.

NuBus Addressing

NuBus addressing requires computing the address from the byte addresses given above under VMEbus Addressing. The formula is:

NuBus byte address = (VMEbus byte address * 2) – 1

All addresses are in IP I/O space.

All byte data is still transferred on data lines D7..D0.

Word addresses on the NuBus are the same as for VMEbus.

Interrupt mapping is a function of the selected carrier board. See your IP carrier board User Manual for more information.

ISA (PC-AT) Bus Addressing

The address map of the IP-16ADC on the ISA bus is given in the Figure below. All addresses are in IP I/O space. Byte accesses are on data lines D7..D0. This byte is the even byte in Intel family host architectures and the odd byte in Motorola 68K host architectures. Word accesses are on data lines D15..D0.

Register Name	ISA Address	Access
Control and Status	$00	Word, R/W
A/D Data Reg	$04	Word, R
Vector Reg	$08	Byte, R/W
Conversion Req Trig	$0C	any, W

Figure 3 ISA Bus Address Map

See section Programming below for register details.

Interrupt mapping is a function of the selected carrier board. See your IP carrier board User Manual for more information.

Programming

Reading this Section

Signals with names having an * (asterisk) suffix are called ACTIVE LOW signals and are TRUE when they are at a 0 logic level which is nominally less than 0.8 Volts. They are FALSE at a 1 logic level which is nominally 1.4 volts or greater. Signals without the suffix are called ACTIVE HIGH signals and their TRUE and FALSE definitions are the OPPOSITE of the ACTIVE LOW definition. For example SWRESET* would be set TRUE by writing a 0 to its bit position which would measure as 0 volts on the IP-16ADC board circuitry.

The phrase "Logic Interface" refers to the Electrical/Logical interface between an Industry Pack board like the IP-16ADC and the carrier board on which it is installed.

The phrase "I/O Interface" refers to the I/O connector on the Industry Pack that carries I/O signals and special ±15 volt power to the Industry Pack through the carrier board.

Please note that operation of the IP-16ADC REQUIRES that the special 15 volt external reference be connected. The IP-16ADC WILL NOT RUN without this reference.

Programmers writing low level drivers for the IP-16ADC are encouraged to refer to Figure 1 near the beginning of this Manual, and to use copies of the Appendix A Worksheet at the end of the Manual. Most modes of the IP-16ADC are selected by setting bits in the 16-bit Control Register. The Appendix A Worksheet is a useful aid in programming this register.

General

All software programmable IP-16ADC board registers should be reinitialized following power up or a Logic Interface reset as the contents are not guaranteed. Control register bits typically power up to logic 0.

Control register bits shown with the same names for both reading and writing have "read back" capability. Other bits have either read or write capability only, or read a signal that is functionally related to the write signal of the same bit.

Caution: The IP-16ADC does not check data width on read and write cycles. If the wrong width is used, proper operation may not result. In particular, all writes to the Control Register must be word wide.

Caution**: The IP-16ADC requires external +15 V and –15V power supplies. Without these, the IP will respond to accesses but the A/D converter will not function. Conversion data will not be valid.**

Control and Status Register

Data Bit #	15	14	13	12	11	10	9	8
Write:	CHGINTEN	DATINTEN	SWRESET*	–	–	–	CRS/FIN*	FREERUN*
Read:	CHGINTEN	DATINTEN	STDBY*	SDL*	CHGINTRQ*	DATINTRQ*	CRS/FIN*	FREERUN*

Figure 4 Control and Status Register Definition, Bits 15..8

Data Bit #	7	6	5	4	3	2	1	0
Write:	ADCH1/2*	BP/UP*	UNITY/HALF*	INSL1	INSL0	CHSL2	CHSL1	CHSL0
Read:	ADCH1/2*	BP/UP*	UNITY/HALF*	INSL1	–	–	–	–

Figure 5 Control and Status Register Definition, Bits 7..0

NOTE: All bits are read/write unless shown with a – in the Figures above. In the following bit definitions an [R] indicates read only or a [W] indicates write only.

Bit [0] CHSL0 [W]
Least significant bit (LSB), Odd/Even Input multiplexer channel select bit. If the inputs are configured in differential mode, the three channel select bits increment through the eight differential input pairs. If the inputs are configured in single ended mode, the three channel select bits increment through the eight Odd (1, 3, 5, 7, 9, 11, 13, 15) or eight Even (2, 4, 6, 8, 10, 12, 14, 16) individual inputs. The CHSL0 bit has an additional function when the inputs are configured for ground or Vref input calibration. In that mode, setting CHSL0 to 0 selects analog ground while setting it to 1 selects Vref. All inputs selected with the channel select bits are applied to the instrumentation amplifier before being digitized by the A/D converter. These bits are write only because it is assumed any routine requesting a conversion would "know" which input channel is being used. See the Input Configuration Map figure below.

Bit [1] CHSL1 [W]
Odd/Even Input multiplexer channel select bit.

Bit [2] CHSL2 [W]
Odd/Even Input multiplexer most significant channel select bit.

Bit [3] INSL0 [W]
Input Configuration Multiplexer least significant select bit (LSB). There are four possible Input configurations selected by INSL bits zero and one as shown below.

Bit [4] INSL1 [R/W]
Input Configuration Multiplexer most significant select bit (MSB). Note that the EVEN and ODD Channel designations are for Single Ended input mode.

INPUT CONFIGURATION	INPUT	INSL1	INSL0	CHSL2	CHSL1	CHSL0
GROUND or CALIBRATION Voltage	AGND	0	0	X	X	0
	VREF	0	0	X	X	1
8 ODD Channels (1 - 15)	CH 1	0	1	0	0	0
	CH 3	0	1	0	0	1
	CH 5	0	1	0	1	0
	CH 7	0	1	0	1	1
	CH 9	0	1	1	0	0
	CH 11	0	1	1	0	1
	CH 13	0	1	1	1	0
	CH 15	0	1	1	1	1
8 EVEN Channels (2 - 16)	CH 2	1	0	0	0	0
	CH 4	1	0	0	0	1
	CH 6	1	0	0	1	0
	CH 8	1	0	0	1	1
	CH 10	1	0	1	0	0
	CH 12	1	0	1	0	1
	CH 14	1	0	1	1	0
	CH 16	1	0	1	1	1
8 DIFFERENTIAL Channels	CH 1	1	1	0	0	0
	CH 2	1	1	0	0	1
	CH 3	1	1	0	1	0
	CH 4	1	1	0	1	1
	CH 5	1	1	1	0	0
	CH 6	1	1	1	0	1
	CH 7	1	1	1	1	0
	CH 8	1	1	1	1	1

Figure 6 Input Configuration Map

Bit [5] UNITY/HALF* [R/W]
Gain selection bit. An input gain of one (unity) is selected by setting this bit to 1. A value of 0 selects a gain of one half. A setting of 1 accommodates up to a 5 volt range. A setting of 0 is required for a range of up to 10 volts. NOTE: An overload situation is created by applying an input voltage greater than 5.5 volts when operating in UNITY mode. The overload will not damage the IP-16ADC, but can raise amplifier temperatures slightly (approximately 10°C) until the overload is removed.

See the table in the Figure 7 below for the relationship between input range and the state of this bit.

Bit [6] BP/UP* [R/W]
A/D Input polarity selection bit. When set to 1, this bit selects bipolar input polarity. A value of 0 selects unipolar input polarity. With a setting of 1, a positive or negative input voltage can be digitized. A setting of 0 properly digitizes only positive voltages. Voltage polarity is defined relative to analog ground where a voltage greater than zero is positive. The ODD channel (CH 01, 03, etc...) of differential inputs pairs is considered the positive input of the pair.

See the figure below for relationship between input range and the state of this bit.

INPUT RANGE	BP/UP*	U/H*
0 to 10 V	0	0
0 to 5 V	0	1
–10 to +10 V	1	0
–5 to +5 V	1	1

Figure 7 Input Range Map

Bit [7] ADCH1/2* [R/W]
A/D input channel select bit. When set to a 0, the AIN2 analog input of the A/D converter is selected. A setting of 1 selects the AIN1 analog input channel. Since AIN2 receives the input signals from the multiplexers, this bit is normally left set to 0. The AIN1 input channel is connected to analog ground without passing through the instrumentation amplifier and may be used for user calibration procedures.

Bit [8] FREERUN* [R/W]
Continuous capture enable. If this bit is true (set to 0) prior to a software or external conversion request, then the conversion request will start Continuous mode conversions at the maximum rate until FREERUN* is set false. Setting FREERUN* false (set to 1) AFTER the falling edge of SDL* will result in one more conversion because FREERUN* arms the conversion at the falling edge of SDL*.

Bit [9] CRS/FIN* [R/W]
Manual coarse or fine tracking mode selection bit. Generally the user will not need to manipulate this bit and it should be set to fine mode (set to 0). When set to a 1, the A/D is forced into the fast and coarse input signal tracking. This may be useful for speeding the A/D's acquisition of a signal that is known to have recently undergone a large (several volt) change in value. However, for accurate conversions, the A/D must have been in fine mode (bit 9 set to 0) for at least 6 A/D clock cycles. This bit MUST be held in fine mode DURING conversion. The SDL* status signal should be used to determine the A/D's state for proper timing of the use of this bit. See the A/D's data sheet for a more detailed description of the bit's use.

Bit [10] DATINTRQ* [R]
Data Available Interrupt status bit. This bit reports the value of the Industry Pack Logic Interface signal INTREQ0*. When set to 0 it indicates that this interrupt is true and pending software service. If enabled, this interrupt becomes true when conversion data is available or an A/D calibration cycle has been completed. The latter case is recognized because the software will have previously issued a SWRESET*. The Data Available Interrupt becomes true (read as 0) on the trailing edge of SDL* or STDBY* and is reset to false when DATINTEN is made false (set to 0).

Bit [11] CHGINTRQ* [R]
Change Window Interrupt status bit. This bit reports the value of the Industry Pack Logic Interface signal INTREQ1*. When set to 0 it indicates that this interrupt is true and pending software service. If enabled, this interrupt becomes true when a conversion has begun and it is appropriate to change the input channel configuration without needing to wait for various settling times to elapse. In other words, changes made immediately after this interrupt occurs do not interrupt the continuous acquisition pipeline. The Change Window Interrupt becomes true (a value of 0) on the leading edge of SDL* is reset to false when CHGINTEN is made false (set to 0).

Bit [12] SDL* [R]
The Serial Data Latch signal indicates the A/D status. At the leading or falling edge of the SDL* signal, the A/D begins shifting out the digital conversion data with the MSB first. At the SDL* signal's trailing edge (SDL* changes from 0 to 1) the data is latched into the output register and is ready to be read by software. The SDL* signal indicates the current A/D status if polled rather than interrupt operation is chosen. The results of the previous conversion may be read while SDL* is a 0 but incorrect data will be read if SDL* changes from a 0 to a 1 while the software is reading the data register. This bit takes 6 clock cycles to go low after the start convert command is issued. Fast processors may poll this bit before it has gone low, resulting in the previous conversion's data being read. In this case, the processor should look for the bit to go low, then wait for it to go high before reading the data. See the timing diagram in Figure 13 on page 26.

Bit [13] SWRESET* [W]
When set true (set to 0), SWRESET* resets the A/D converter. When SWRESET* becomes false (1), an internal A/D calibration cycle is automatically initiated. This bit is set to 0 by a Logic Interface reset and must be set to 1 by a software write to the Control Register.

Bit [13] STDBY* [R]
The calibration cycle status bit for the A/D. The A/D drives this bit to 0 during a calibration cycle. Completion of the calibration cycle is indicated by this bit changing from a 0 to a 1.

Bit [14] DATINTEN [R/W]
The Data Interrupt Enable bit. Setting this bit true (1) allows the DATINTRQ* signal to assert a data available interrupt at the Industry Pack Logic interface. Setting this bit false (0) forces the DATINTRQ* signal to stay false until DATINTEN is again made true. Generally, if interrupts are to be used, DATINTEN is made true prior to initiating a conversion.

Bit [15] CHGINTEN [R/W]
The Change Window Interrupt Enable bit. Setting this bit true (1) allows the CHGINTRQ* signal to assert a change window interrupt at the Industry Pack Logic interface. Setting this bit false (0) forces the CHGINTRQ* signal to stay false until CHGINTEN is again made true. If interrupts are to be used, CHGINTEN is made true prior to initiating a conversion.

Interrupt Vector

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	-	-	-	-	-	-	V7	V6	V5	V4	V3	V1	V1	V0
Read	-	-	-	-	-	-	-	-	V7	V6	V5	V4	V3	V1	V1	V0

Figure 8 Interrupt Vector Register

The IP-16ADC stores any desired eight bit interrupt vector in this register. On a Write cycle, only D7...D0 are stored with the value of D15...D8 being ignored. On a read cycle, the previously stored value of D7...D0 is read back upon the same bits as they were written. Only byte access is recommended for the vector register.

A/D Data Register

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Read	O15	O14	O13	O12	O11	O10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0

Figure 9 A/D Data Register

A read from this address reads the data from the A/D converter.

Conversion Request Trigger

Writing to this address initiates an immediate A/D conversion. There is no associated data register. All reads from this address are ignored. Data written has no affect. A data value of $FFFF is recommended to reduce noise caused by data bus switching.

ACQUISITION MODES

There are two conversion modes that can be triggered from two sources. The availability of the resulting digitized value of the input signal can be determined in two ways.

The two conversion modes are Single and Continuous conversion. In Single mode a conversion trigger results in a single A/D conversion. In Continuous mode a conversion trigger starts a series of conversions. The first conversion is followed by additional conversions at the maximum A/D conversion rate. The Control register FREERUN* bit determines the conversion mode.

The two trigger sources are software and external. The software trigger is simply a write to the Conversion Request register. The external trigger has the same functionality as the software trigger, but occurs when the signal on the I/O Interface External Conversion pin is brought to a logic 0. This pin must be driven with a device that can sink 4.2 milliamps to ground (logic 0) or source 3.4 volts at 50 microamps (logic 1). Typical interface logic devices can easily meet these requirements. The external conversion signal must not be true longer than 63 A/D clock cycles (7.874 microseconds) per conversion and thus it must toggle on and off for each trigger event. The two trigger sources are logically OR'd so if no external conversion is desired the I/O pin input can be tied to a logic 1 level or left open.

Note that the CONVERSION REQUEST TRIGGER virtual register is write only. A read from it has no effect.

The digitized data is always read from the A/D Data Register. If it is desired to indicate data availability by interrupt, the user must write an interrupt vector to the Interrupt Vector Register

and enable the Data Interrupt by setting the Control register DATINTEN bit to 1. This will enable an INTREQ0* on the Industry Pack Logic Interface when the A/D output data register receives the conversion results. That interrupt's service routine should read the data value and then clear the interrupt by making DATINTEN false.

Data availability can always be determined, regardless of interrupt usage, by reading the control register status bit SDL*. When this bit changes from a 0 to a 1, a new data value has just been determined and transferred to the data register.

Note that the A/D output data register is read only. A write to it has no effect.

In Continuous conversion mode, the A/D output data register is updated at the end of every conversion regardless of software access to the output data register. If more than one conversion cycle has elapsed since the output data register was read, all but the most recent value is lost. To guarantee the output data register is not read during the very brief interval (<50 nanosecond) during which it is updated, it is recommended that the data register be read immediately after a data available interrupt or immediately after the SDL* bit changes from 0 to 1. To verify that SDL* has not changed state during the data register read, it is recommended that the data register read be followed by another read of the Control register SDL* bit.

CHANGING INPUT SOURCE and CONFIGURATION

The A/D chip used on the IP-16ADC board requires 15 A/D clock cycles, worst case, to acquire and track its input signal PRIOR to a conversion request. That takes 1.5 microseconds for an eight MHz A/D clock rate chip. The first six clock cycles perform a fast, coarse acquisition followed by nine clock cycles of slow, fine acquisition. If this acquisition is shortened by software manipulation of the CRS/FIN bit, conversion accuracy may suffer for time varying signal inputs.

Changing the input channel and input configuration can result in transient error voltages being added to the input signal and producing erroneous conversion results. Waiting at least a 3.5 microsecond settling time from the last configuration change, will ensure the transients have died out and the signal is stable and ready for conversion. This settling time can be pipelined into the normal conversion process if the channel and configuration changes are made immediately following the start of the internal hold of the input signal by the A/D converter. Doing so removes the impact of the change on conversion throughput.

There are two mechanisms for determining when to perform configuration changes so they will be pipelined and not affect performance. The first method is to monitor the Control register SDL* bit and perform the changes immediately after it changes from 1 to 0 at the beginning of a conversion. The second method is to use the Change Window Interrupt which will provide an interrupt when the SDL* signal changes from a 1 to a 0. Using either method, the software has 3.5 microsecond (28 A/D clock cycles, which yields more time with slower A/D chips) to complete the channel and configuration changes. Multiplexer changes should always be performed first as they have the longest settling times.

If it is desired to determine the Change Window by interrupt, the user must verify a valid interrupt vector has been loaded into the Interrupt Vector register and then enable the Change Window Interrupt by setting the Control register CHGINTEN bit to 1. This will enable an INTREQ1* on the Industry Pack Logic Interface when the SDL* signal begins indicating the beginning of the change window. That interrupt's service routine should complete the channel and configuration changes within 3.5 microseconds (see above) and then clear the interrupt by making CHGINTEN false.

NOTE: The short times available for transparent configuration changes are due to the high speed of the IP-16ADC. Fast processors running optimized code will be necessary to fully benefit from the IP-16ADC's speed.

Accuracy

In any analog circuit there are many factors that determine its overall accuracy. Only a few of these factors must be understood by the user for effective use of the IP-16ADC. This section provides some basic discussion of accuracy.

For more detailed information refer to the manufacturer's data sheets for the input multiplexers, the differential amplifiers and the A/D chip. The Engineering Kit provides a cable, a terminal block, technical documentation, and reprints of data sheets for all major ICs on the IP-16ADC.

The design and layout of the IP-16ADC minimizes the effects of digital switching noise on the analog to digital conversion process. However, host processor read or write accesses made to the registers of the IP-16ADC while a conversion is in progress may introduce small errors in the conversion result. The greatest accuracy is achieved by avoiding all host processor accesses to the IP after a conversion is started. The Data Available interrupt can be used to signal the end of the conversion rather than polling the Control and Status register.

DC Accuracy

There are two errors that affect basic DC accuracy. The first is zero error, or "offset." This is the error that the A/D makes when reading its own analog ground on single-ended, or shorted differential input terminals. This error is corrected by subtracting the known error from all readings.

The second error is gain error. Gain error is the difference between the ideal gain and the actual gain of the instrumentation amplifier, track and hold, and A/D, after offset is corrected. Gain error is corrected by multiplying readings by a correction factor. The closer the correction factor is to one, the less the gain error. Gain error is always corrected after the offset correction.

There are separate offset and gain correction factors for each of the two gain settings and each of the two input modes supported by the IP-16ADC. Thus there are a total of eight calibration values. Only two of these are used to correct any one reading.

Analog to digital converters are sometimes specified by both their uncorrected and their corrected accuracy. Since it is expected that the IP-16ADC will always be used in the corrected mode, only the corrected accuracy is specified. Information on uncorrected accuracy may be obtained from the manufacturer's data sheets and by contacting GreenSpring Computers. The typical corrected accuracy is specified as plus or minus one LSB over temperature on all gain settings, after software calibration.

Factory calibration values are stored in the ID PROM on the IP-16ADC. These values may be used to correct A/D readings. Even greater accuracy can be achieved by performing software calibration prior to taking a reading. The main advantage of the software calibration is compensation for the current operating temperature. Software calibration takes advantage of the very high precision (2 ppm/C typical) voltage reference on the IP. This voltage and analog ground are software selectable as inputs for digitization. The same calibration voltage is used for both gain settings. The calibration algorithm measures offset and gain error on each of the two gain settings, storing these values in RAM. The software routine that reads the A/D then uses these recently computed RAM based correction factors instead of the factory generated correction factors stored in the ID-PROM.

Some A/D chips suffer from errors in addition to offset and gain. This error is usually called differential non-linearity. (If the error is linear, then the two standard correction factors will always provide complete correction.) The differential non-linearity of the IP-16ADC is plus or minus one half LSB; this error is included in the overall accuracy specification of the IP-16ADC. This differential non-linearity specification guarantees that the IP-16ADC will have no missing digital counts or codes.

For more information see the Calibration section, refer to the manufacturer's data sheets for individual components, or contact GreenSpring Computers.

Settling Time

Settling time for the IP-16ADC is primarily a function of the input multiplexers. See the section Changing Input Source and Configuration for more information about settling time. Input sensors that have a very high impedance may require additional settling time due to cable and IP-16ADC input capacitance.

Track and Hold

An internal track and hold circuit is provided to aid in accurately measuring time varying signals. The IP-16ADC automatically changes from track to hold mode when a conversion is initiated. When a sampled (held) value is not being converted, the A/D is tracking the analog input.

The re-acquisition of a time varying analog input following a conversion begins with a brief coarse acquisition followed by continuous fine tracking until the next conversion request. The coarse acquisition tracks the input to within one percent within six clock cycles and then switches to fine tracking mode which requires an aditional nine clock cycles to exactly track the input. While the A/D chip must be left in fine mode while performing a conversion, at other times the coarse or fine tracking states may be selected as desired by software. The CRS/FIN control register bit selects the state.

Manipulating the tracking might be necessary with peculiar inputs or timing requirements, but it is seldom necessary to do so. Please refer to the A/D chip documentation for further details.

Calibration

HARDWARE CALIBRATION

A calibration cycle is automatically performed by the A/D chip every time the reset pin of the chip changes from a 0 to a 1. Following calibration, the A/D chip is specified as having a typical accuracy of ±1 LSB (±3 LSB worst case) over the 0 to 70°C temperature range.

> ***This calibration can take several seconds to complete. For the CS5101A it takes 11,528,160 A/D clock cycles (4 or 8 MHz A/D clock). For the CS5102A it takes 2,882,040 A/D clock cycles (1.6 or 2 MHz A/D clock). The standard IP-16ADC uses an 8 MHz CS5101A which requires 5.76 seconds for calibration.***

The A/D reset can be generated from two sources. The first is an Industry Pack Logic Interface RESET* signal. The second is the Control register SWRESET* signal. Either of these signals becoming a logic 0 begins the reset cycle, with their return to a logic 1 terminating the reset and beginning the calibration cycle. The Industry Pack Logic Interface RESET* signal resets the Control register SWRESET* bit to the active state (0). This Control register bit will remain active until software writes the Control register with a 1 in the SWRESET* bit, Control register bit position 13.

The completion of the calibration cycle is indicated by the Control register STDBY* status bit changing from a 0 to a 1. The data available interrupt can be generated by this event, signaling calibration completion, if it is enabled AFTER the SWRESET* bit is brought back to a logic 1. Since a Logic Interface reset also clears the IP-16ADC interrupt enables, STDBY* can not use the interrupt and must be polled following that reset source.

A/D chip calibration cycles may be initiated whenever desired. After board warm up and following known ambient temperature changes would be typical calibration opportunities. It does not matter whether calibration is performed in Bipolar or Unipolar mode.

SOFTWARE CALIBRATION

This section describes how to use the calibration data stored in the ID PROM. All correction data in the ID PROM is stored in units of 1/4 LSB. The correction numbers are signed 16-bit words. This section also outlines a method of performing software calibration.

The Ideal Case

If there were no analog errors whatsoever, then the following would be true. The goal of the correction factors and following algorithm is to get as close to this ideal as possible.

1. The on board reference would produce exactly +5.000 and –5.000 volts.

2. Full scale for the ADC is defined as 65,536 counts. For bipolar operation zero is defined as 32,768 ($8000). Note that since the maximum sixteen bit number is 65,535 ($FFFF) that the maximum achievable output reading is one LSB less than the maximum voltage stated in the ideal range. An output of zero from the ADC represents the most negative voltage in the range.

3. For the IP-16ADC, one LSB is defined as the voltage span of the full scale range divided by 65,536.

Range	Span	One LSB
0 to +5 V	5 V	76.2939 µV
–5 to +5 V	10 V	152.5879 µV
0 to +10 V	10 V	152.5879 µV
–10 to +10 V	20 V	305.1758 µV

Figure 10 IP-16ADC Resolution

Unipolar Correction Formula

The best way to understand the complete correction formula for the IP-16ADC is to follow the process of correcting errors one at a time. This example begins with the unipolar case. The basic equation to calculate the calibrated voltage is as follows:

$$(1) \quad V = (Offset\ compensated\ value - Gain\ compensated\ value) \times \left(\frac{Range}{65536}\right)$$

The Offset compensated value is just the value read from the IP-16ADC minus the offset calibration value. The Gain calibration value stpred in the ID Prom is the deviation from the true value at the maximum count in relation to 0 volts. Since the Gain compensated value is independent of the Offset compensated value, the offset calibration value must be subtracted from the value read from the IP-16ADC. In order to find the Gain compensated value, take the value read from the IP-16ADC, subtract the offset calibration value stored in the IP Prom and multiply the result by the Gain calibration value divided by 65536.

Equation (1) now looks like this:

$$(2) \quad V = \left((ADC - Offset) - \left((ADC - Offset) \times \frac{Gain}{65536}\right)\right) \times \left(\frac{Range}{65536}\right)$$

Where ***V*** is the corrected voltage measured by the IP-16ADC at its input. ***ADC*** is the number produced by the IP-16ADC (in the range 0 to 65,535). ***Offset*** and ***Gain*** are the correction factors stored in the PROM, normalized to bits. ***Range*** is the maximum voltage minus the minimum voltage possible at the input to the ADC.

The Offset and Gain values stored in the ID PROM are in units of 1/4 LSB. The equation must have these values divided by 4. The equation for correcting Unipolar readings is:

$$(3) \quad V = \left(\left(ADC - \frac{Offset}{4}\right) - \left(\left(ADC - \frac{Offset}{4}\right) \times \frac{\left(\frac{Gain}{4}\right)}{65536}\right)\right) \times \left(\frac{Range}{65536}\right)$$

Bipolar Correction Formula

When a Bipolar range is used, equation (2) must be modified to compensate for the zero volts reference point since zero volts is now at a count of 32,768. The value (***ADC***) read from the IP-16ADC must have 32,768 subtracted from it. The gain correction coefficient, which is stored as the number of bits of correction to be applied to a full scale IP-16ADC reading, as if there were no zero offset, must also be corrected for the zero offset count. Therefore values read from the IP-16ADC and corrected for Offset errors must be multiplied proportionately by the Gain correction value divided by the full scale count value. The full scale count value is 32,768 for Bipolar ranges. Equation (2) now becomes:

$$(4)\quad V = \left(\left(ADC - 32768 - Offset \right) - \left(\left(ADC - 32768 - Offset \right) \times \left(\frac{Gain}{32768} \right) \right) \right) \times \frac{Range}{65536}$$

It must be remembered that the Offset and Gain values stored in the ID PROM are in units of 1/4 LSB. The equation must have these values divided by 4. The equation for correcting Bipolar ADC readings is:

$$(5)\quad V = \left(\left(ADC - 32768 - \frac{Offset}{4} \right) - \left(\left(ADC - 32768 - \frac{Offset}{4} \right) \times \frac{\left(\frac{Gain}{4} \right)}{32768} \right) \right) \times \left(\frac{Range}{65536} \right)$$

Software Calibration Algorithm

The following procedure outlines a method for calculating the Offset and Gain correction factors for the IP-16ADC. For this example, the IP-16ADC is programmed to operate in Unipolar mode with Half gain which supports an input rage of 0 to +10 volts. All addresses given below are VMEbus addresses.

1. Configure the IP-16ADC to digitize the analog ground in Unipolar mode with Half gain by writing $2100 to the Control and Status Register (IP slot base address + $00).

2. Write $FFFF to the Conversion Request Register (IP slot base address + $0C) to start a conversion.

3. Delay 11 microseconds for the conversion to complete.

4. Read the conversion results from the A/D Data Register (IP slot base address + $04).

5. Repeat steps 2 through 4 100 to 1000 times and average the readings.

6. The average value calculated in step 5 is the Offset correction factor.

7. Configure the IP-16ADC to digitize the reference voltage in Unipolar mode with Half gain by writing $2101 to the Control and Status Register (IP slot base address + $00).

8. Write $FFFF to the Conversion Request Register (IP slot base address + $0C) to start a conversion.

9. Delay 11 microseconds for the conversion to complete.

10. Read the conversion results from the A/D Data Register (IP slot base address + $04).

11. Repeat steps 8 through 10 100 to 1000 times and average the readings.

12. Subtract the Offset correction factor calculated in step 5 from the average value calculated in step 11.

13. Divide the reference value calculated in step 13 by the value of the reference in counts. Since the reference is a near perfect 5.00V, this value is 32768.

14. The value calculated in step 14 is the Gain correction factor.

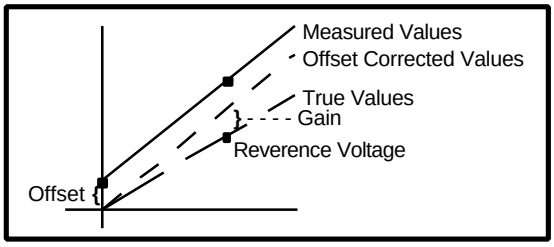

Figure 11 Offset and Gain Correction of Data

ID PROM

Every IP contains an IP PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto-configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires a particular revision IP, it may check for it directly.

Standard data in the ID PROM on the IP-16ADC is shown in Figure 12 below. For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from GreenSpring Computers. The ID PROM is implemented in the IP-16ADC internally as an 82S123 16-pin socketed DIP.

The location of the ID PROM in the host's address space is dependent on the carrier used. Normally for VMEbus carriers the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one.

3F	Calibration: 10V range bipolar gain Low Byte	
3D	Calibration: 10V range bipolar gain High Byte	
3B	Calibration: 10V range unipolar gain Low Byte	
39	Calibration: 10V range unipolar gain High Byte	
37	Calibration: 5V range bipolar gain Low Byte	
35	Calibration: 5V range bipolar gain High Byte	
33	Calibration: 5V range unipolar gain Low Byte	
31	Calibration: 5V range unipolar gain High Byte	
2F	Calibration: 10V range bipolar offset Low Byte	
2D	Calibration: 10V range bipolar offset High Byte	
2B	Calibration: 10V range unipolar offset Low Byte	
29	Calibration: 10V range unipolar offset High Byte	
27	Calibration: 5V range bipolar offset Low Byte	
25	Calibration: 5V range bipolar offset High Byte	
23	Calibration: 5V range unipolar offset Low Byte	
21	Calibration: 5V range unipolar offset High Byte	
1F		
1D		
1B		
19		
17	CRC for bytes used	(XX*)
15	No of bytes used	(20)
13	Driver ID, high byte	(00)
11	Driver ID, low byte	(04)
0F	reserved	(00)
0D	Revision	(C0)
0B	Model No IP-16ADC	(36)
09	Manufacturer ID GreenSpring	(F0)
07	ASCII "C"	(43)
05	ASCII "A"	(41)
03	ASCII "P"	(50)
01	ASCII "I"	(49)

Figure 12 ID PROM Data (hex)

* The CRC includes the calibration data and therefore is not constant from IP to IP. The CRC is the least significant eight bits of the FCS as described in CCITT T.30 (Fascicle VII.3) section 5.3.7.

Timing

The standard IP-16ADC uses the 8 MHz IP-CLK as the A/D converter clock (ADCLK). A conversion requires 64 clocks. The signal *DONE*, internal to a PAL, goes high (true) 7 clocks after SDL* goes high or after Reset* goes high.

In Single Conversion mode, a write to the Conversion Request Trigger virtual register causes Software Convert (*SWCNV*) to become active. This signal is internal to the PAL on the IP. The signal *SWCNV* causes *ARMED* to become active. When both *DONE* and *ARMED* are active, HOLD* is made active to start a conversion. The SDL* line goes low 6 clocks into the conversion to indicate the start of the shifting of serialized conversion results out of the A/D converter and into the input stage of the Data register. At the end of the conversion, SDL* goes high and transfers the conversion results from the input stage of the Data register to the output stage for reading by the software.

Once Continuous Conversion mode is set by writing a zero in bit 8, FREERUN*, of the Control and Status register, nothing happens until a conversion is triggered by writing to the Conversion Request Trigger register. Writing to this address starts the first Continuous Conversion. The SDL* line goes low 6 clocks into the conversion to indicate the start of the shifting of serialized conversion results out of the A/D converter and into the input stage of the Data register. This high to low transition of SDL* is used to clock the *ARMED* signal internal to the PAL to the active state. At the end of the conversion, SDL* goes high and transfers the conversion results from the input stage of the Data register to the output stage for reading by the software. This low to high transition of SDL* starts a 7 clock delay which ends with *DONE* becoming active. Once both *DONE* and *ARMED* are active, HOLD* is made active to start the next Continuous Conversion mode conversion. There is an 8 clock gap between the end of one conversion and the start of the next conversion. This process continuous until a one is written to bit 8, FREERUN*, of the Control and Status register.

The Change Window Interrupt (CHANGEINTRQ* on the schematic, CHGINT* in the timing diagrams below) is clocked active by the high to low transition of the SDL* signal from the A/D converter. This occurs 6 clocks after the conversion is started. The end of the conversion is signaled by SDL* going high. This low to high transition is used to clock the Data Available Interrupt active (DATAINTRQ* on the schematic, DATINT* in the timing diagrams below). These interrupts are reset by the interrupt service software disabling and then enabling the interrupt during the interrupt service.

The input multiplexers require a minimum of 3.5 microseconds to stabilize after selecting a new channel. The change should be made as close as possible to the high to low transition of SDL*. Changing the multiplexer between the time a conversion is triggered and the time that SDL* goes low may corrupt the conversion. If the IP-16ADC is operating in Continuous Conversion mode, a new conversion is automatically started 8 clocks after SDL* goes high. If the input multiplexer is change too close to the end of a conversion cycle, the input will not be stable when the automatically triggered next conversion is started.

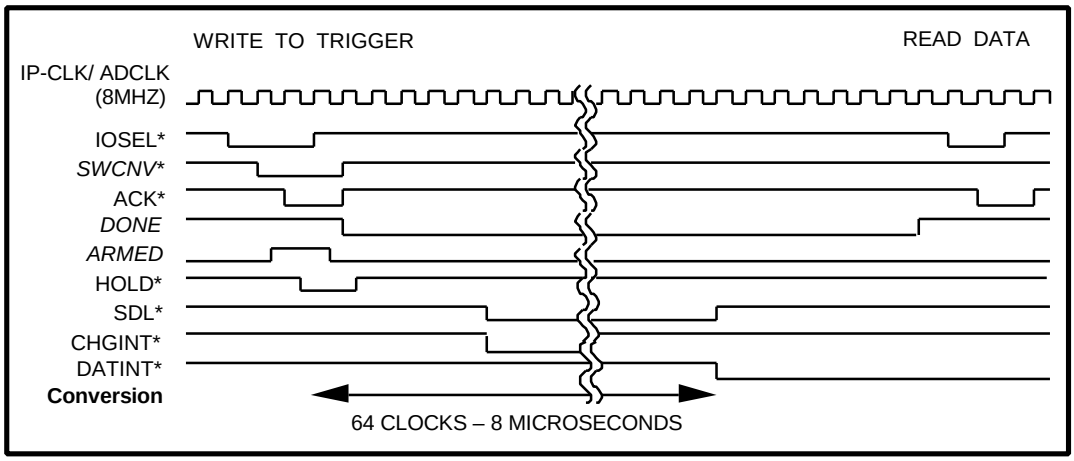

Figure 13 Single Conversion Cycle Timing

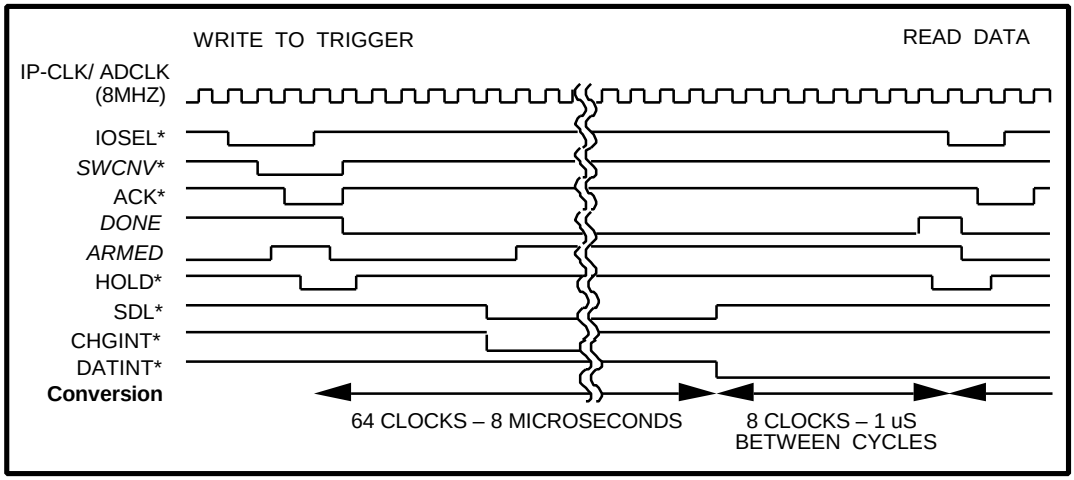

Figure 14 Continuous Conversion Cycle Timing

Differential Input Mode

The differential input mode of the IP-16ADC is not a floating input. Engineers who are interfacing sensors to this IP must not use a conventional hand held DVM as a model for interfacing to the IP-16ADC.

Differential inputs have two requirements that floating inputs do not:

- The input must be within the common mode range of the IP
- The input must have a galvanic ground return connection to establish the necessary small bias current needed by the input instrumentation amplifier.

The traditional way to meet both of these requirements is to connect a nominal ground from the sensor (or sensor amplifier or signal conditioner) to any of the analog ground pin on the IP's I/O. The input bias current requirement can be met in any of several other ways, for example, by connecting one side of the differential sensor output to the ground on the IP (this is often called pseudo-differential) or by connecting a return path to either side of the ±15 volt power supply.

Failure to provide a bias current return path will cause the input circuit of the instrumentation amplifier to be come starved. This will typically result in the following errors: the voltage reading may be accurate at first, then show high drift, finally staying at one rail or the other (readings of 0000 or FFFF in hex). For example, a simple differential two-wire connection of a 1.5 volt battery will not produce a stable reading because there is no galvanic path from the ground on the IP to either side of the battery.

The necessary input bias current is very small, in the nanoampere range. Thus the return path may have moderately high impedance. The chance of a ground loop between separate systems may be avoided by added a series resistor, say 100K? , between the two ground connections.

Figures 15 through 17 on the next page provide examples of how to connect a differential mode sensor to the IP-16ADC. Figure 15 shows a sensor ground wired directly (via an optional series resistor) to the analog ground on the I/O wiring of the IP. Figure 16 shows a connection between the power supply ground of a sensor and the common ground on the external power supplies of the IP. Figure 17 shows a pseudo-differential connection to a floating sensor.

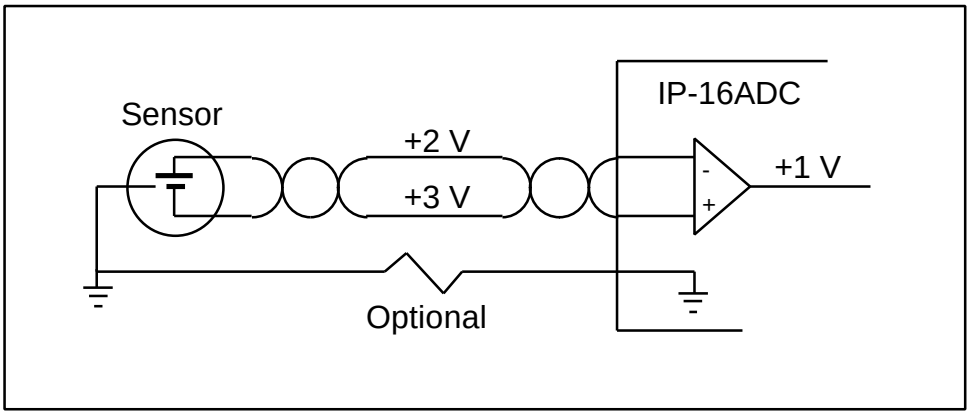

Figure 15 Example Differential Input Wiring

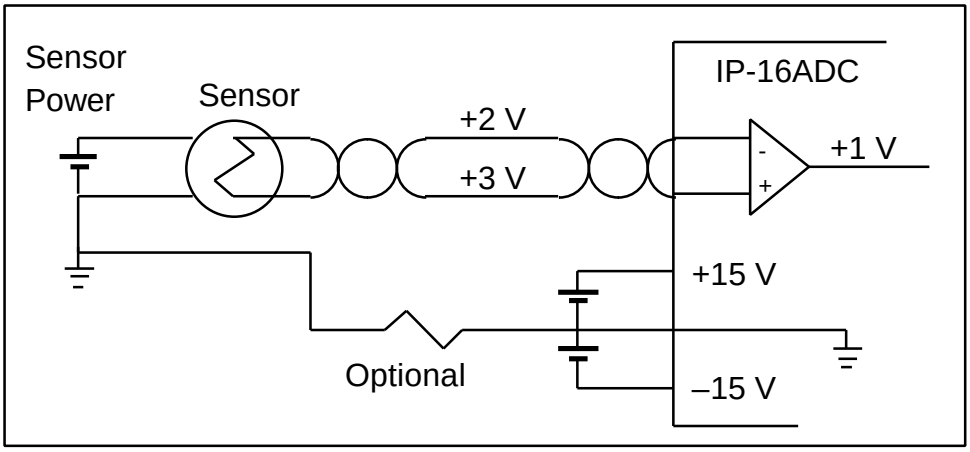

Figure 16 Example Differential Input Wiring

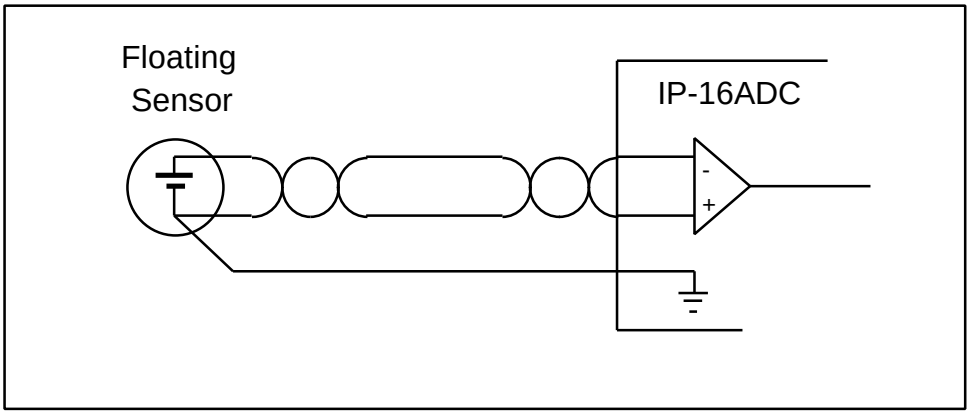

Figure 17 Pseudo-differential Input Circuit

I/O Pin Wiring

This section gives the pin assignments for IP-16ADC.

The pin numbers given in Figures 18 and 19 below correspond to numbers on the 50-pin IndustryPack I/O connector, to the wires on a 50-pin flat cable plugged into a standard IP carrier board, and to the screw terminal numbers on the IP-Terminal block.

I/O Cable Pin Number	Channel Number Differential	Notes	Channel Number Single-Ended
1		Ground	
2	Ch 1+		Ch 1
3		Ground	
4		Ground	
5	Ch 1–		Ch 2
6		Ground	
7		Ground	
8	Ch 2+		Ch 3
9		Ground	
10		Ground	
11	Ch 2–		Ch 4
12		Ground	
13		Ground	
14	Ch 3+		Ch 5
15		Ground	
16		Ground	
17	Ch 3–		Ch 6
18		Ground	
19		Ground	
20	Ch 4+		Ch 7
21		Ground	
22		Ground	
23	Ch 4–		Ch 8
24		Ground	

Figure 18 I/O Pin Assignment First Half

I/O Cable Pin Number	Channel Number Differential	Notes	Channel Number Single-Ended
25		Ground	
26	Ch 5+		Ch 9
27		Ground	
28		Ground	
29	Ch 5–		Ch 10
30		Ground	
31		Ground	
32	Ch 6+		Ch 11
33		Ground	
34		Ground	
35	Ch 6–		Ch 12
36		Ground	
37		Ground	
38	Ch 7+		Ch 13
39		Ground	
40		Ground	
41	Ch 7–		Ch 14
42		Ground	
43		**Ground**	
44		External Convert* Command	
45		**+ 15 V Input Power**	
46		**– 15 V Input Power**	
47	Ch 8+		Ch 15
48		Ground	
49		Ground	
50	Ch 8–		Ch 16

Figure 19 I/O Pin Assignment Second Half

NOTE: An external ±15 volt power supply must be connected to the I/O interface of the IP-16ADC for proper operation.

IndustryPack Logic Interface Pin Assignment

Figure 20 below gives the pin assignments for the IndustryPack Logic Interface on the IP-16ADC. Pins marked n/c below are defined by the specification, but not used on IP-16ADC. See also your User Manual for your IP Carrier board for more information.

GND	GND	1	26
CLK	+5V	2	27
Reset*	R/W*	3	28
D0	IDSel*	4	29
D1	n/c	5	30
D2	MEMSel*	6	31
D3	n/c	7	32
D4	INTSel*	8	33
D5	n/c	9	34
D6	IOSel*	10	35
D7	n/c	11	36
D8	A1	12	37
D9	n/c	13	38
D10	A2	14	39
D11	n/c	15	40
D12	A3	16	41
D13	IntReq0*	17	42
D14	A4	18	43
D15	IntReq1*	19	44
n/c	A5	20	45
n/c	n/c	21	46
n/c	n/c	22	47
n/c	Ack*	23	48
+5V	n/c	24	49
GND	GND	25	50

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 20 Logic Interface Pin Assignment

Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-16ADC is constructed out of 0.062 inch thick FR4 V0 material. The six copper layers consist of two signal layers on the top and bottom, and four internal layers. Two internal layers are dedicated to power and ground planes. Two additional layers are used for signal wiring. The internal ground planes are separated into digital ground and analog ground. These planes are connected at the ADC IC. The precision analog grounds are all run on separate traces to a single analog star ground, which is then connected to the analog ground close to the combined analog digital ground connection point. The star ground wiring is on an internal dedicate plane section. This design eliminates almost all ground loops.

Spaces on all layers between traces are copper filled. All copper filled islands are then connected to the appropriate analog or digital ground, creating numerous small faraday shields. Approximately 11 separate ground planes may be counted internal in the IP-16ADC. This design minimized noise throughout the circuit. The large amount of copper on all layers also acts as a significant heat sink, causing the components on IP-16ADC to run at the same temperature, minimizing temperature gradient induced errors and drift.

Through hole and surface mounting of components is used. IC sockets use gold plated, screw-machine pins. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IndustryPack connectors are keyed, shrouded and gold plated on both contacts and receptacles. They are rated at 1 Amp per pin and 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured to the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.

Warranty and Repair

GreenSpring Computer warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, GreenSpring Computer's sole responsibility shall be to repair, or at GreenSpring Computer's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to GreenSpring Computers. All replaced products become the sole property of GreenSpring Computers.

GreenSpring Computer's warranty of and liability for defective products is limited to that set forth herein. GreenSpring Computers disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

GreenSpring's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of GreenSpring Computers, Inc.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. GreenSpring Computers will not be responsible for damages due to improper packaging of returned items. For service on GreenSpring Products not purchased directly from GreenSpring Computers contact your reseller. Products returned to GreenSpring Computers for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
GreenSpring Computers
1204 O'Brien Drive
Menlo Park, CA 94025
(415) 327-1200
(415) 327-3808 fax

Specifications IP-16ADC

This section gives the technical specification for the standard grade IP-16ADC.

Size	Single-high IndustryPack®
Number of A/D channels	16 single ended, or 8 differential, dynamically mixable, additional internal channels for calibration
A/D resolution	16 bits
A/D input voltage ranges	The four ranges are software selectable –10 V to +10 V bipolar 0 V to +10 V unipolar –5 V to +5 V bipolar 0 V to +5 V unipolar
Conversion rate	100 K samples/sec continuous, 8 µs conversion time
Settling time	2 µsec to 0.01% (instrumentation amp), typical
Input impedance	60 M? (instrumentation amp) Approximately 5 pF plus carrier board wiring. plus 2K? in series with 55 pF
Input crosstalk	68 db typical from input multiplexer @ f=100KHz
Input voltage protection	±65 VDC with power on ±80 VDC with power off
Common mode rejection	91 db at 60 Hz (instrumentation amp), typical 80 db @ 60 Hz (instrumentation amp), min Common mode voltage range is ±12 volt typical, ±11 volts minimum.
Basic Accuracy	16 bit Guaranteed no missing codes
Non linearity	0.002% (instrumentation amp), maximum 0.0002% (instrumentation amp), typical 0.002% (A/D converter), maximum ±0.25 bit DNL 3 sigma (A/D converter),typical S/D >100 db typical @ 1 KHz, (A/D converter), typical
Noise	0.65 LSB typical one sigma, reading internal voltage reference, in system with switching power supplies 92 db S/N (A/D converter), typical 90 db S/N (A/D converter), maximum 35 µV rms unipolar mode, (A/D converter), typical 70 µV rms bipolar mode, (A/D converter), typical
Internal voltage reference	5.012 volts ±.01%
Calibration voltages	0 volts (local analog ground) 4.99894 volts nominal

2.49947 volts nominal
(by using internal divide by two)

A/D calibration	Factory calibrated voltage reference. ADC is self-calibrating. Gain and offset first order errors removed by host software.
Calibration voltage drift	1 ppm/°C typical 2 ppm/°C maximum
Wait states	Zero, read One, write
Convert Command	Software trigger, external trigger, or free-run
Interrupt	Vectored Interrupt on end of conversion
LSI	Crystal Semiconductor CS5101-KL8
Dimensions	1.8 by 3.9 by 0.340 inches
External power supply	±15 volt external supply required
Power requirements	+5 VDC, 210 mA typical, 270 mA max +15 VDC, 45 mA typical, 70 mA max –15 VDC, 45 mA typical, 70 mA max
External power supply	external ±15 volt supply required. ±12 volts may be used for 5 V input ranges only (some specifications may be reduced).
Test conditions	20°C, typical
Environmental	Operating temperature: 0 to 70°C Humidity: 5 - 95% non-condensing Storage temperature: –10 to +85°C

Specifications IP-16ADC-LC

This section gives the technical specification for the -LC low cost grade IP-16ADC.

Size	Single-high IndustryPack®
Number of A/D channels	16 single ended, or 8 differential, dynamically mixable, additional internal channels for calibration
A/D resolution	16 bits
A/D input voltage ranges	The four ranges are software selectable –10 V to +10 V bipolar 0 V to +10 V unipolar –5 V to +5 V bipolar 0 V to +5 V unipolar
Conversion rate	50 K samples/sec continuous, 16 µs conversion time
Settling time	2 µsec to 0.01% (instrumentation amp), typical
Input impedance	60 M? (instrumentation amp) Approximately 5 pF plus carrier board wiring. plus 2K? in series with 55 pF
Input crosstalk	68 db typical from input multiplexer @ f=100KHz
Input voltage protection	±55 VDC with power on ±35 VDC with power off
Common mode rejection	91 db at 60 Hz (instrumentation amp), typical 80 db @ 60 Hz (instrumentation amp), min Common mode voltage range is ±12 volt typical, ±11 volts minimum.
Basic Accuracy	15 bit Guaranteed no missing codes (16 bit)
Non linearity	0.01% (instrumentation amp), maximum 0.0003% (instrumentation amp), typical 0.003% (A/D converter), maximum
Noise	0.65 LSB typical one sigma, reading internal voltage reference, in system with switching power supplies 90 db S/N (A/D converter), typical 87 db S/N (A/D converter), maximum 35 µV rms unipolar mode, (A/D converter), typical 70 µV rms bipolar mode, (A/D converter), typical
Internal voltage reference	5.012 volts ±.01%
Calibration voltages	0 volts (local analog ground) 4.99894 volts nominal 2.49947 volts nominal (by using internal divide by two)

A/D calibration	Factory calibrated voltage reference. ADC is self-calibrating. Gain and offset first order errors removed by host software.
Calibration voltage drift	2 ppm/°C typical 5 ppm/°C maximum
Wait states	Zero, read One, write
Convert Command	Software trigger, external trigger, or free-run
Interrupt	Vectored Interrupt on end of conversion
LSI	Crystal Semiconductor CS5101-JL16
Dimensions	1.8 by 3.9 by 0.340 inches
External power supply	±15 volt external supply required
Power requirements	+5 VDC, 210 mA typical, 270 mA max +15 VDC, 45 mA typical, 70 mA max –15 VDC, 45 mA typical, 70 mA max
External power supply	external ±15 volt supply required. ±12 volts may be used for 5 V input ranges only (some specifications may be reduced).
Test conditions	20°C, typical
Environmental	Operating temperature: 0 to 70°C Humidity: 5 - 95% non-condensing Storage temperature: –10 to +85°C

Appendix A—Control Register Programming Worksheet

Data Bit #:		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write:		CHG IINT EN	DAT INT EN	SW RESET*	-	-	-	CRS / FIN*	FREE RUN*	ADCH 1/2*	BP / UP*	UNITY / HALF*	IN SL1	IN SL0	CH SL2	CH SL1	CH SL0
Read:	**HEX Value**	CHG IINT EN	DAT INT EN	STDBY*	SDL*	CHG IINT RQ*	DAT INT RQ*	CRS / FIN*	FREE RUN*	ADCH 1/2*	BP / UP*	UNITY / HALF*	IN SL1	-	-	-	-
Unity, BP, AGND, CH = n/a	21E0	0	0	1	x	x	x	0	1	1	1	1	x	x	x	x	x
Half, UP, AGND, CH = n/a	2100	0	0	1	x	x	x	0	1	0	0	0	0	0	x	x	0
Half, UP, VREF, CH = n/a	2101	0	0	1	x	x	x	0	1	0	0	0	0	0	x	x	1
Half, BP, EVEN, CH = 6	2152	0	0	1	x	x	x	0	1	0	1	0	1	0	0	1	0
Half, BP, DIFF, CH = 2	215A	0	0	1	x	x	x	0	1	0	1	0	1	1	0	1	0